UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,831	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030479US1	6642

35525 7590 01/27/2006

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,831	DEWITT ET AL.	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/03, 7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, declaration, and information disclosure statement, all filed 30 September 2006; additional information disclosure statement filed 1 July 2005.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

4. Applicant is requested to fill in the blank spaces on pages 1-2 of the specification with the now-assigned application serial numbers.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 1, 6 and 23 are objected to because of the following:

Claim 1: The examiner asserts that if the indicator is located in the instruction as described on page 27 of the specification and fig. 5 of the drawings, all instructions must perform an interrupt. If the indicator is located next to the instruction in the instruction packet, the indicator is, by default, associated with the instruction purely by location. Since each instruction has an indicator associated with it (as in Fig. 5), each instruction will cause an interrupt. Causing an interrupt for every instruction appears to be an undesired outcome of the invention. Examiner suggests amending claim 1 to replace "associated with the instruction" with a phrase indicating that the indicator must signal that an interrupt *should* occur during the processing of the instruction, not simply if the indicator is associated with the instruction.

Claim 6, line 3: Any bit in the bundle that is being used is not a spare bit. Hence, using one or more bits as an indicator renders them no longer spare. Examiner recommends removing "spare" from the claim and will interpret the claim as such.

Claim 23, line 2: "includes" should read "include"

Appropriate correction is required.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 21-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Pages 64-65 of the specification define "computer readable media" to include "transmission-type media". Transmission media are not tangible, and hence, non-statutory.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-5 and 8-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Heisch (U.S. Patent No. 5,774,724).

10. As per claim 1, Heisch discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction for execution in an instruction cache (Fig. 2 cache 60) in a processor in the data processing system, determining whether an indicator is associated with the instruction (Col. 5 lines 58-65); and forcing an interrupt if the indicator is associated with the instruction (Col. 5 line 66 – col. 6 line 6).

11. As per claim 2, Heisch discloses the method of claim 1, wherein the forcing step comprises: sending a signal from an instruction cache to an interrupt unit in the processor; and processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit. (Col. 6 lines 2-6) *The examiner asserts that logic comparing the current instruction's address to the address stored in the IAB register constitutes part of the instruction cache. The logic must inherently generate a signal to alert the interrupt handler to a pending interrupt. If no such signal was generated, the interrupt would go unprocessed.*

12. As per claim 3, Heisch discloses the method of claim 2, wherein the processing step includes: executing code associated with the interrupt. (Col. 6 line 9-13) *The examiner asserts that when control is transferred to another function, code is executed which is associated with that function.*

13. As per claim 4, Heisch discloses the method of claim 3, wherein the code records cache misses by a functional unit attempting to access instructions in a cache. (Col. 6 lines 21-25) *The examiner asserts that counting cache misses constitutes recording.*

14. As per claim 5, Heisch discloses the method of claim 1, wherein the indicator is located in a shadow memory. (Col. 5 lines 58-65) *The examiner asserts that the IAB register is not located in main memory, and hence, constitutes shadow memory.*

15. As per claim 8, Heisch discloses a method in a data processing system for processing data, the method comprising: responsive to an access of data, determining whether an indicator is associated with the data (Col. 5 lines 58-65); and generating an interrupt if the data is associated with the indicator. (Col. 5 line 66 – col. 6 line 6) *The examiner asserts that the method described by Heisch anticipates causing an interrupt on a data access (Col. 10 line 13-15).*

16. As per claim 9, Heisch discloses the method of claim 8, wherein the generating step comprises: generating a signal by a data cache in which the data is located; and receiving the signal generated by the data cache at an interrupt unit, wherein the signal indicates a presence of the interrupt to the interrupt unit. (Col. 6 lines 2-6) *The examiner asserts that logic comparing the current access address to the address stored in the IAB register constitutes part of the data cache. The logic must inherently generate a signal to alert the interrupt handler to a pending interrupt. If no such signal was generated, the interrupt would go unprocessed.*

17. As per claim 10, Heisch discloses the method of claim 8 further comprising: processing the interrupt in an interrupt unit in response to generation of the interrupt. (Col. 6 line 2-6)

18. As per claim 11, Heisch discloses the method of claim 10, wherein the processing step comprises: executing a code for handling the interrupt. (Col. 6 line 9-

13) *The examiner asserts that when control is transferred to another function, code is executed which is associated with that function.*

19. As per claim 12, Heisch discloses the method of claim 8, wherein the indicator is associated with the data through a specific value in a memory location for the data. (Col. 5 lines 58-65) *The examiner asserts that the address of interest loaded into the IAB register is a memory location. Col. 10 line 13-15 dictates that the address can be that of data.*

20. As per claim 13, Heisch discloses the method of claim 8, wherein the data is located in a memory location. *The examiner asserts that an address inherently points to a location in memory.*

21. As per claim 14, Heisch has taught a processing system performing the method of claim 1, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 1 above.

22. As per claim 15, Heisch has taught a processing system performing the method of claim 2, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 2 above.

23. As per claim 16, Heisch has taught a processing system performing the method of claim 3, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 3 above.

24. As per claim 17, Heisch has taught a processing system performing the method of claim 4, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 4 above.

25. As per claim 18, Heisch has taught a processing system performing the method of claim 8, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 8 above.

26. As per claim 19, Heisch has taught a processing system performing the method of claim 9, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 9 above.

27. As per claim 20, Heisch has taught a processing system performing the method of claim 10, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 10 above.

28. As per claim 21, Heisch has taught a computer program product performing the method of claim 1, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 1 above.

29. As per claim 22, Heisch has taught a computer program product performing the method of claim 2, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 2 above.

30. As per claim 23, Heisch has taught a computer program product performing the method of claim 3, consequently claim 23 is rejected for the same reasons set forth in the rejection of claim 3 above.

31. As per claim 24, Heisch has taught a computer program product performing the method of claim 8, consequently claim 24 is rejected for the same reasons set forth in the rejection of claim 8 above.

32. As per claim 25, Heisch has taught a computer program product performing the method of claim 9, consequently claim 25 is rejected for the same reasons set forth in the rejection of claim 9 above.

33. Claims 1, 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Short (Short, K. L. "Embedded Microprocessor Systems Design: An Introduction Using the Intel 80C188EB." Prentice-Hall, Inc: 1998. Page 761.)

34. As per claim 1, Short discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether an indicator is associated with the instruction; and forcing an interrupt if the indicator is associated with the instruction. *The examiner asserts that if the opcode of the instruction (indicator) indicates the Interrupt instruction (Short pg. 761), an interrupt will be forced.*

35. As per claim 6, Short discloses the method of claim 1, wherein the instruction is received in a bundle and wherein the indicator comprises at least one bit in a field in the bundle. *The examiner asserts that a bundle may contain just one instruction: Further, the opcode (indicator) comprises at least one bit in a field in the instruction, which is in the bundle.*

36. As per claim 7, Short discloses the method of claim 1, wherein the indicator is located in a field in the instruction. *The examiner asserts that the opcode (indicator) comprises at least one bit in a field in the instruction.*

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Frank et al. (U.S. Patent No. 5,822,578) disclose a system in which instructions inject interrupts into a processing stream for the purpose of debug and performance monitoring.

38. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100